

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re patent application of

Bruce B. Doris et al.

Confirmation No.: 6189

Serial No.: 10/695,748

Group Art Unit: 2814

Filed: October 30, 2003

Examiner: T. Le

For: STRUCTURE AND METHOD TO ENHANCE BOTH nFET and pFET
PERFORMANCE USING DIFFERENT KINDS OF STRESSED LAYERS

Commissioner for Patents
PO Box 1450
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APPELLANT'S REPLY BRIEF UNDER 37 C.F.R. §41.41

This reply brief is in reply to the Examiner's Answer mailed November 6, 2007, as supplemented by the supplemental action mailed November 29, 2007.

The Examiner does not identify any new grounds of rejection in the Examiner's Answer. However, it is respectfully submitted that the errors in the ground of rejection asserted in the final action in this application are particularly evident from the Examiner's assertions and response to Appellants arguments as stated in the Examiner's Answer.

Specifically, in the last line of page 3 of the Examiner's Answer, in rejecting sole independent claim 10, the Examiner asserts that Hachimine et al. teaches a shear force isolation layer 15, making reference to paragraph 0170 of Hachimine et al. This reference to paragraph 0170 is the only reference made in the Examiner's Answer to disclosure of properties of layer 15 or the purpose for which layer 15 is provided and

the passage is, in fact, silent in regard to any stress isolation properties or function of layer 15 other than as an insulator. The Examiner does not make any reference in the Examiner's Answer to any other references to layer 15 in Hachimine et al. such as paragraph 0207 which specifically and explicitly discloses use of insulating film 15 as "an etching stopper upon removal of the silicon nitride film 14b"; the etching which stops on layer 15 being necessitated to achieve *selective* placement of layer 14b *only* over the PFET of Hachimine et al. (just as layer 14a is selectively placed *only* over the NFET (also by etching) and to prevent overlap of layers 14a and 14b in the completed device such that the opposite tensile and compressive forces of layers 14a and 14b, respectively, do not interact to reduce the forces applied to either of the transistor channels, as discussed in paragraph 214 of Hachimine et al. As was pointed out in Appellants' Brief (which the Examiner does not answer), it is again respectfully pointed out that, *in accordance with the present invention, as claimed*, such etching and the function of an etch stop would be unnecessary if layer 15 *could* function as a "stress isolation layer" since such stress isolation would prevent any such interaction of forces; allowing tensile and compressive layers to remain overlapped in the completed device.

Consistent therewith, paragraphs 0279 - 0280 of Hachimine et al. describe an embodiment (Figure 31) where the tensile and compressive layers are, in fact, allowed to overlap in the completed device with one of the tensile or compressive layers being used to modify (e.g. reduce) the effects of the other; an effect which can only be achieved if layer 15 *does not isolate the forces in the overlapping stressed layers* and which necessarily *relies upon such forces being transferred* between the stressed layers and to the substrate. Other passages clearly indicating that Hachimine et al. does not disclose shear force isolation properties for layer 15 and does not recognize the possibility of deriving such properties or function from layer 15 are noted on pages 13 and 14 of Appellants' Brief which the Examiner similarly has not answered.

Thus it is clearly seen that Hachimine et al. *does not even contemplate* any stress isolation properties of layer 15, as the Examiner *assumes*, or even recognize the possibility of a material having such properties much less the use of such a material to simplify the manufacturing process for transistors of different conductivity types on a common substrate having enhanced channel carrier mobility. The Examiner continues the erroneous assertion of layer 15 being a shear force isolation layer throughout the discussion of the rejection of the dependent claims.

In response to arguments on this issue in the Appellants' Brief, the Examiner not only fails to answer many of the arguments grounded in explicit teachings of Hachimine et al. that are completely inconsistent with layer 15 being a "shear force isolation layer", as discussed above, but provides only two reasons for disagreement therewith on pages 5 and 6 of the Examiner's Answer. It is respectfully submitted that neither of these reasons is substantively, logically or procedurally correct or defensible.

First, the Examiner notes that the disclosed "shear force isolation layer" (identified in the drawings by reference numerals 12 and 120 with which material 12 may be replaced) is only disclosed to be a dielectric or insulator and thus suggests that layer 15 of Hachimine et al. which is also an insulating material could thus be equivalently referred to by the same terminology. This assertion is respectfully submitted to be incorrect since the shear force isolation properties of the layer are described at many occurrences in the specification such as page 11, first full paragraph, where deposition of an oxide by high density plasma deposition is disclosed to result in a material which can serve as *both* an etch stop *and* a neutral barrier between stressed layers or page 12, first full paragraph, which explicitly indicates layer 120 "serves to isolate stresses from later applied layers from reaching the substrate". The Examiner's assertion is also illogical, particularly as applied to Hachimine et al. which makes no reference to shear force isolation by a layer of

material and, in fact, assumes the absence of such a property in most disclosed embodiments and actually *relies* upon the absence of such a property in the embodiment of Figure 31 in which layers 14a and 14b are allowed to remain overlapped in the completed device in order to obtain *reduction* of the force applied by one of the two stressed layers, as disclosed in paragraphs 279 - 280, as noted above. Therefore, it is respectfully submitted that even a nominal reference to layer 15 as a "shear force isolation layer" is completely unjustified as being inconsistent with and even contrary to the actual content of Hachimine et al. and would, in fact, be misdescriptive thereof. Such nomenclature contrary to the actual content of the reference relied upon, particularly when asserted as a basis for justifying a rejection for anticipation, cannot be supported by the structures being capable of functioning as an insulator and an etch stop; both of which properties and functions are very different from functioning to isolate shear forces.

Second, the Examiner asserts that since the structures of Hachimine et al. and the invention appear to be identical (notwithstanding the fact that the structures asserted to appear identical other than the embodiment of Figure 31 are *intermediate* manufacturing states and not the final device and which would not function in the manner intended for the completed device and the fact that such Figures and the descriptions thereof, at best, merely teach a general correspondence of layers but not the *constitution* or *properties* of the layer between the stressed layers as anything other than an insulator and an etch stop) thus justifying a presumption of inherency of a shear force isolation function or property. As pointed out above, Hachimine et al. does not disclose layer 15 to be anything other than an insulator and etch stop while the explicit disclosure of Hachimine et al. is inconsistent with and contrary to the "shear force isolation" property claimed which the Examiner clearly ignores in making such an assertion of the structures appearing to be identical. In this regard, it is again respectfully pointed out that inherency for purposes of anticipation is

necessarily incorrect if it must be *presumed*. Rather, inherency for purposes of anticipation is only proper where that which is not disclosed but considered to be inherent logically, necessarily and unavoidably flows from subject matter which is, in fact, disclosed in the reference relied upon. In this case, the claimed “shear force isolation” property which the Examiner asserts to be inherent is, in fact, inconsistent with or even contrary to that which is disclosed in Hachimine et al. and therefore an assertion of inherency, particularly for the reasons asserted by the Examiner, is not only unjustified but clearly improper.

Therefore, it is clearly seen that neither of the reasons stated by the Examiner for insisting that layer 15 of Hachimine et al. is a “shear force isolation layer” is logically or substantively defensible. The claims at issue are clearly structural claims rather than product-by-process claims and the Examiner’s assertions in this regard are not even procedurally defensible to shift the burden of proof of demonstrating a difference to Applicants upon mere assertion by the Examiner that claimed structures appear substantially identical (which difference, in any case, has, in fact, been demonstrated in the response filed December 13, 2005, by submission of articles teaching application or communication of stress through forms of silicon oxide, thus clearly negating any proper assertion of inherency).

In summary, throughout the entire prosecution of this application, the Examiner has continually failed to make a *prima facie* demonstration of anticipation of any claim. Each and every attempt by the Examiner to justify attribution of a shear force isolation function to layer 15 of Hachimine et al.; which function or property is not, in fact, disclosed therein, has been fully refuted and the Examiner has provided no viable rationale for continuing to make such an unsupported attribution, even in the Examiner’s Answer. The Examiner’s asserted conclusions as to the content of Hachimine et al., regardless of how the Examiner may attempt to justify them, can only be reached through attribution of disclosed features of the present invention to

the reference which are not contained in but are contrary to the actual content of the reference relied upon. The reference relied upon simply does not contain the teachings the Examiner attributes to it or support any assertion of inherency in regard to a shear force isolation layer, however the Examiner may seek to justify the assertions made, an no *prima facie* demonstration of anticipation based on Hachimine et al. has been or can be made. Accordingly, it is respectfully submitted that the Examiner's continued adherence to the sole ground of rejection under 35 U.S.C. §102 based on Hachimine et al. is clearly in error and reversal of the Examiner is respectfully requested.

Respectfully submitted,



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